CLAIMS

What is claimed is:

1. A method for forming a semiconductor structure, comprising:
providing a semiconductor substrate;
forming a first tunnel dielectric overlying the semiconductor substrate;
forming a first floating gate overlying the first tunnel dielectric;
depositing a plurality of pre-formed discrete elements over the first floating gate;
forming a control dielectric overlying the plurality of pre-formed discrete elements; and
forming a control gate overlying the control dielectric.

2. The method of claim 1, further comprising:
forming an isolation trench in the semiconductor substrate;
filling the isolation trench with a trench fill material;
forming a second tunnel dielectric overlying the semiconductor substrate; and
forming a second floating gate overlying the second tunnel dielectric, wherein the trench fill material is between the first floating gate and the second floating gate.

3. The method of claim 2, wherein depositing the plurality of pre-formed discrete elements over the first floating gate further comprises depositing the plurality of pre-formed discrete elements over the trench fill material and the second floating gate.

4. The method of claim 3, wherein forming the control dielectric is performed such that the control dielectric overlies the plurality of pre-formed discrete elements overlying the first floating gate, the trench fill material, and the second floating gate.

5. The method of claim 1, wherein depositing the plurality of pre-formed discrete elements over the first floating gate comprises:
forming at least one of the plurality of pre-formed discrete elements during a gas phase nucleation, and

after forming the at least one of the plurality of pre-formed discrete elements, attaching the at least one of the plurality of pre-formed discrete elements to a surface of the semiconductor substrate over the first floating gate.

6. The method of claim 5, wherein the gas phase nucleation is performed in a first chamber and the attaching is performed in a second chamber.

7. The method of claim 6, wherein the attaching is performed using forces selected from the group consisting of electrostatic forces and thermophoretic forces.

8. The method of claim 1, wherein the first floating gate comprises polysilicon.

9. The method of claim 1, wherein the first floating gate comprises metal.

10. The method of claim 1, wherein forming the control dielectric comprises forming an oxide layer overlying the plurality of pre-formed discrete elements and forming a nitride layer overlying the oxide layer.

11. The method of claim 1, wherein forming the control dielectric comprises forming a dielectric layer having a high dielectric constant overlying the plurality of pre-formed discrete elements.

12. The method of claim 1, wherein the plurality of pre-formed discrete elements are further characterized as pre-fabricated discrete elements.

13. The method of claim 1, wherein the plurality of pre-formed discrete elements comprise nanocrystals.

14. The method of claim 1, wherein the plurality of pre-formed discrete elements comprise discrete storage elements.

15. The method of claim 1, wherein each of the plurality of pre-formed discrete elements comprise a substantially conductive material.

16. The method of claim 1, wherein after depositing the plurality of pre-formed discrete elements, each of the plurality of pre-formed discrete elements is spaced apart from each other by at least 10 nanometers on average.

17. A method for forming a semiconductor structure, comprising:
providing a semiconductor substrate;
forming a first tunnel dielectric overlying the semiconductor substrate;
forming a first floating gate overlying the first tunnel dielectric;
forming a first interfacial layer overlying the first floating gate;
forming a plurality of discrete elements over the first interfacial layer;
forming a control dielectric overlying the plurality of discrete elements; and
forming a control gate overlying the control dielectric.

18. The method of claim 17, further comprising:
forming an isolation trench in the semiconductor substrate;
filling the isolation trench with a trench fill material;
forming a second tunnel dielectric overlying the semiconductor substrate;
forming a second floating gate overlying the second tunnel dielectric; and
forming a second interfacial layer overlying the second floating gate, wherein the trench fill material is between the first floating gate and the second floating gate.

19. The method of claim 18, wherein forming the plurality of discrete elements over the first interfacial layer further comprises depositing the plurality of pre-formed discrete elements over the trench fill material and the second interfacial layer.

20. The method of claim 19, wherein forming the control dielectric is performed such that the control dielectric overlies the plurality of discrete elements overlying the first floating gate, the trench fill material, and the second floating gate.

21. The method of claim 17, wherein the first floating gate comprises one of polysilicon and metal.

22. The method of claim 17, wherein the plurality of discrete elements comprise nanocrystals.

23. The method of claim 17, wherein the plurality of discrete elements comprise discrete storage elements.

24. The method of claim 17, wherein each of the plurality of discrete elements comprise a substantially conductive material.

25. The method of claim 17, wherein forming the plurality of discrete elements over the first interfacial layer is performed using a process selected from the group consisting of low pressure chemical vapor deposition (LPCVD), physical vapor deposition (PVD), and atomic layer deposition (ALD).

26. The method of claim 17, wherein after depositing the plurality of discrete elements, each of the plurality of discrete elements is spaced apart from each other by at least 10 nanometers on average.

27. The method of claim 17, wherein forming a first interfacial layer overlying the first floating gate comprises forming an oxide layer overlying the first floating gate.

28. The method of claim 17, wherein forming a first interfacial layer overlying the first floating gate comprises forming a metal layer overlying the first floating gate.

29. A semiconductor structure, comprising:
a semiconductor substrate;
a first tunnel dielectric overlying the semiconductor substrate;
a first floating gate overlying the first tunnel dielectric;
a plurality of discrete elements over the first floating gate, wherein each of the plurality of discrete elements are spaced apart from each other;
a control dielectric overlying the plurality of discrete elements; and
a control gate overlying the control dielectric.

30. The semiconductor structure of claim 29, further comprising an interfacial layer overlying the first floating gate and underlying the plurality of discrete elements.

31. The semiconductor structure of claim 29, further comprising:
an isolation trench filled with a trench fill material;

a second tunnel dielectric overlying the semiconductor substrate; and

a second floating gate overlying the second tunnel dielectric, wherein the trench fill material is between the first floating gate and the second floating gate.

32. The semiconductor structure of claim 31, wherein the plurality of discrete elements overlie the trench fill material and the second floating gate.

33. The semiconductor structure of claim 29, wherein the first floating gate comprises polysilicon.

34. The semiconductor structure of claim 29, wherein the first floating gate comprises metal.

35. The semiconductor structure of claim 29, wherein the plurality of discrete elements comprise nanocrystals.

36. The semiconductor structure of claim 29, wherein the plurality of discrete elements comprise discrete storage elements.

37. The semiconductor structure of claim 29, wherein each of the plurality of discrete elements comprise a substantially conductive material.

38. The semiconductor structure of claim 29, wherein each of the plurality of discrete elements are spaced apart from each other by at least 10 nanometers.